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# Development of FELIX based readout system for HV-CMOS sensor testbeam

**W. Wu,**[a,1] **H. Chen,**[a] **K. Chen,**[a] **F. Lanni,**[a] **H. Liu,**[a] **L. Xu,**[a] **M. Benoit,**[b] **G. Lacobucci**[b] **and M. Vicente Barrero Pinto**[b]

[a] *Brookhaven National Laboratory, PO Box 5000, Upton, NY 11973, U.S.A.*
[b] *Département de Physique Nucléaire et Corpusculaire (DPNC), University of Geneva, 24 quai Ernest Ansermet, 1211 Geneève 4, Switzerland*

*E-mail:* weihaowu@bnl.gov

Abstract: The High Voltage CMOS (HV-CMOS) sensors are extensively investigated by the ATLAS collaboration for the High-Luminosity LHC (HL-LHC) upgrade of the Inner Tracker (ITk) detector. The HV-CMOS technology is a commercial integrated circuit process with the advantages of monolithic readout and fast charge collection. A front-end test platform of CaRIBOu (Control and Readout Itk BOard) and a testbeam Telescope based on the ATLAS IBL (Insertable B-Layer) silicon pixel modules, have been developed for the HV-CMOS sensor study and characterization in testbeam experiments. The Front-End LInk eXchange (FELIX) system is a new approach to function as the gateway between detector front-end electronics and the commodity switched network in the ATLAS upgrade. A FELIX based readout system has been developed for both the CaRIBOu and the testbeam Telescope. It has been deployed successfully in the testbeam at the CERN SPS H8 beamline in August 2017. The test results show that the readout system is capable of sensor calibration and readout of a high-density pixel detector with high trigger rate in testbeam experiments.

Keywords: Control and monitor systems online; Data acquisition circuits; Hardware and accelerator control systems; Particle tracking detectors

[1] Corresponding author.

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## 1 Introduction

The ATLAS experiment is planning to build a new all-silicon Inner Tracker (ITk) for the High-Luminosity LHC (HL-LHC), requiring the production of upgraded radiation tolerant pixel detectors [1]. The High Voltage CMOS (HV-CMOS) sensors are promising candidates for multiple advantages compared to the traditional hybrid pixel detectors [2]. The HV-CMOS technology has high resistivity of the substrate, combined with the possibility to apply reverse bias voltage larger than 120 V, allowing the creation of a large depletion zone within the substrate [3]. The depletion area is an n-well/p-type diode, which functions as a pixel sensor element. Its electric field is sufficient to generate fast and large enough signals for charge collection both before and after the irradiation. The CMOS process also allows the integration of CMOS electronics like ampifiers within the collection electrode, which can efficiently increase the electrical signal size. CaRIBOu (Control and Readout Itk BOard) is a front-end modular test system for HV-CMOS sensor characterization [4]. It is developed based on Xilinx ZC706 evaluation boards plus several custom-designed boards. A testbeam Telescope of IBL (Insertable B-Layer) DC (double-chip) modules has also been built for HV-CMOS sensor testbeam experiments [5]. It can be used to track charged particles in the testbeam. The Front-End LInk eXchange (FELIX) is a readout system to interface with front-end electronics and a commodity network in the ATLAS Run 3 and Run 4 upgrade [6–8]. In this paper, a new FELIX based readout system has been developed for both testbeam Telescope and CaRIBOu system with high trigger rate in the testbeam experiment. This readout system is capable of readout FE-I4B calibration data, as well as HV-CMOS sensor data in the testbeam experiment.

## 2 HV-CMOS sensor testbeam

The HV-CMOS sensors have been widely studied for their performance characterization. Several prototypes with different standard CMOS processes have been fabricated like the CCPDv4 (Capacitively Coupled Pixel Detectors) and H35DEMO [9, 10]. The CCPDv4 is produced with the AMS 180 *nm* HV-CMOS process, and the H35DEMO is fabricated in the AMS 350 *nm* HV-CMOS process. The H35DEMO comprises two monolithic matrices and two analogue matrices with a large number of pixels, and a few test structures for sensor characterization, as shown in the figure 1. The monolithic matrices have analogue electronics in the collecting electrode and on-chip digital readout electronics at their periphery. The analogue matrices have analogue readout electronics only in the collecting electrode and a readout ASIC such as the FE-I4B is needed to process and extract the data. Its pixel size is 50 µm × 250 µm which is compatable with the FE-I4B chip [11].

Over the last decades, testbeam experiments using charged particle tracking by beam telescopes are proved usefull for detector sensor characterization like spatial resolution, timing performance and detection efficiency. It can be used to study the response of sensor prototypes to particles with known trajectories. Due to the availability of the FE-I4B readout ASIC, a testbeam Telescope based on six ATLAS IBL modules has been constructed to test small HV-CMOS sensor prototypes that are also called Device Under Test (DUT) at the CERN SPS H8 (180GeV), as shown in the figure 2 [5]. It also combines with centrally managed services like power supplies, cooling system and movable positioning stages. A data acquisition system (DAQ) is also needed to trigger readout of both of the testbeam Telescope and the DUT in the experiment.

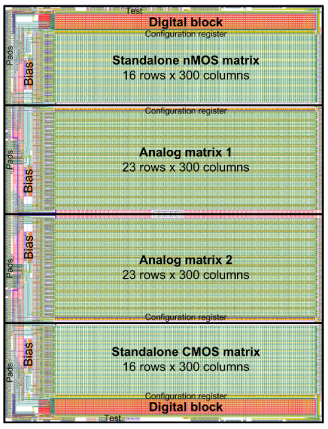


**Figure 1**. Layout of H35DEMO. Reproduced from [10]. © 2016 IOP Publishing Ltd and Sissa Medialab srl.

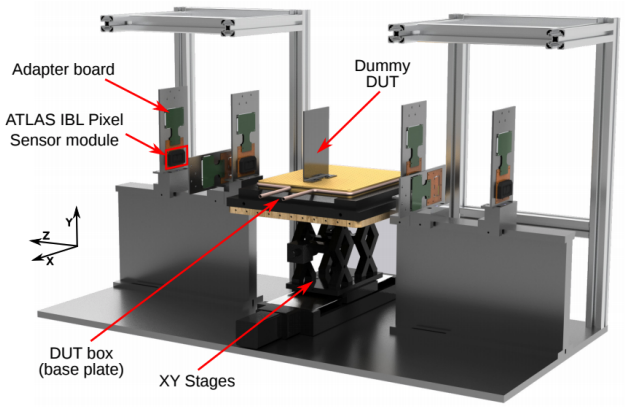


**Figure 2**. Computer generated image of the testbeam Telescope setup. Reproduced from [5]. © 2016 IOP Publishing Ltd and Sissa Medialab srl.

## 3 FELIX

The FELIX is the core of the new Trigger/DAQ architecture in the ATLAS upgrade. It functions as a router between front-end custom serial links and a commodity network in the back-end. Replacing traditional point-to-point links between front-end components and detector specific ROD (ReadOut Driver) systems, FELIX provides scalability, flexibility, uniformity and upgradability. In



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the ATLAS Run 3 upgrade, FELIX will be used by the Liquid Argon (LAr) Calorimeters, Level-1 Calorimeter trigger system, BIS 7/8 and the muon New Small Wheel (NSW) detectors, as shown in the figure 3 [12, 13]. FELIX production board, as shown in the figure 4, is equipped with one 16-lane PCIe Gen3 interface and eight onboard MiniPODs. Each MiniPOD has 12 links connected to FPGA (Field Programmable Gate Array) GTH transceivers, providing 48 bidirectional optical links in total [14]. The optical links between front-ends and the FELIX are GBT (GigaBit Transceiver) links or FULL mode links. The GBT links use CERN GBT protocol which has a line rate of 4.8 Gb/s with FEC (Forward Error Correction) encoding for radiation tolerance. The FULL mode links has a higher data rate, which has a line rate of 9.6 Gb/s with 8b10b encoding. The detector event data can be sent to host server through PCIe interface and then distributed to network.

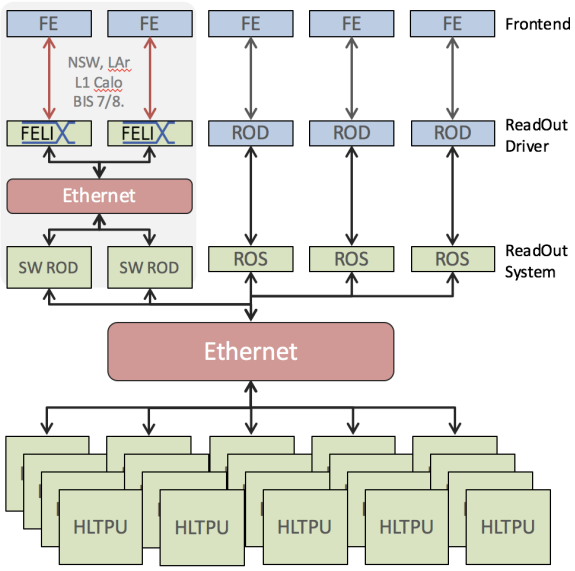


**Figure 3**. FELIX in ATLAS Run 3 upgrade.

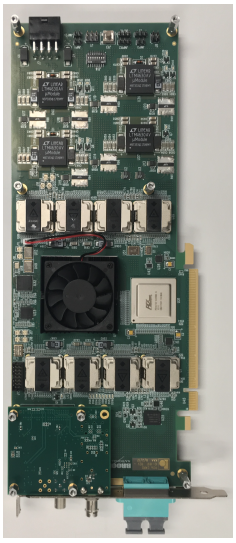

**Figure 4**. FELIX board.

## 4 Hardware

This FELIX based readout system includes two Xilinx ZC706 evaluation boards in the front-end: one for CaRIBOu system readout and the other for testbeam Telescope readout. The block diagram is shown in the figure 5. A Telescope FMC Card was developed as an interface between testbeam Telescope and the ZC706 board. Six RJ45 Cat6 cables are used for connecting IBL DC modules in the testbeam Telescope. There are three optical links between front-end electronics and the FELIX in back-end: one mainly for clock distribution and the other two for data transmission [15]. FELIX software tools are used to issue all the control commands and continuously store all the pixel data for off-line analysis.

### 4.1 CaRIBOu

CaRIBOu is a modular test system for HV-CMOS sensors study. It includes a CaR (Control and Readout) board and a DUT (Device Under Test) board, as shown in the figure 6 and figure 7 [4].



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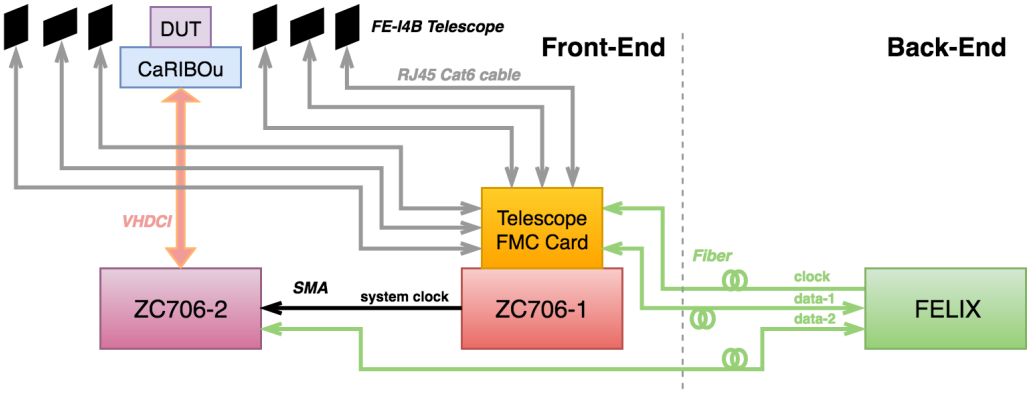


**Figure 5**. Test setup of testbeam Telescope and CaRIBOu readout with the FELIX.

The CaR board provides adjustable power supplies, bias voltages, calibration pulse generators, etc. It is connected to the ZC706 board through a VHDCI (Very High Density Cable Interconnect) cable. In order to reduce the crosstalk and ground loop between the CaR board and the ZC706, all the signals between them are implemented as LVDS differential signals. The DUT board has a front-end readout chip of FE-I4B mounted, together with a HV-CMOS sensor prototype. On the DUT board of H35DEMO, the sensor is capactively coupled to the FE-I4B readout chip using a thin layer of epoxy glue with good uniformity over a large surface. More details about the H35DEMO can be found in [10].

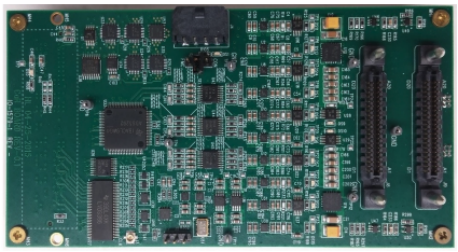

**Figure 6**. CaR board.

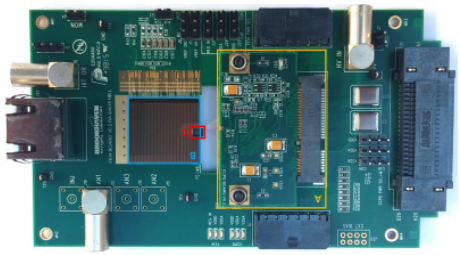

**Figure 7**. DUT board.

### 4.2 Telescope FMC card

The Telescope FMC Card, as shown in the figure 8, functions as an interface between IBL DC modules in the testbeam Telescope and the ZC706 board. This board is connected to the ZC706 through FMC connectors and has an external 12 Volt power supply. It has size of 10 $cm \times 40$ $cm$. Its interface connectors are all placed in the same side. In this case, this Telescope FMC Card, together with one ZC706 board, can be placed in 1U chasis. There are 12 RJ45 ports for connecting to all of the 6 IBL DC modules. Another group of 12 RJ45 ports are reserved for MIMOSA readout [16]. A jitter cleaner chip of Si5345 is implemented on board in order to improve the recovered clock quality from the FELIX GBT link. This clock chip can be configured by the FELIX software tools through the GBT links. One of the output channels is sent to the other ZC706 board in the figure 5 through SMA connectors for clock synchonization of the whole readout system. The LEMO connectors



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on the right of the figure 8 receive HitOr signals from two of the IBL DC modules, which are used for trigger generation in the testbeam experiment. There are 4 SFP connectors for optical links connected to GTX transceiver in the ZC706 FPGA [17]. The Xilinx IBERT tool was used to evaluate the performance of these links, and no error was observed in the line rate of 9.6 Gb/s in more than 24 hours [18]. The I2C buses on the Telescope FMC Card and ZC706 boards can be accessed by FELIX software tools. In this way, users can carry out slow control and monitoring through the FELIX in the back-end. The Telescope FMC Card also has several LVDS repeaters and voltage translators available.

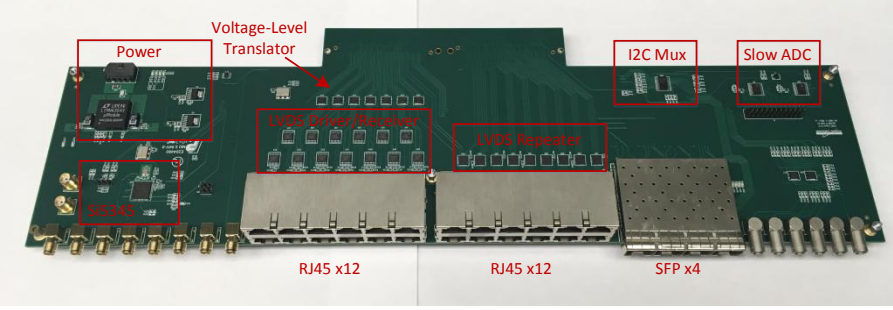


**Figure 8**. Telescope FMC card.

## 5 Firmware

Two Xilinx ZC706 evaluation boards are used in the readout system as shown in the figure 5. The functional block diagram of FPGA firmware is shown in the figure 9. It includes two ZC706 firmwares in the front-end, as well as FELIX firmware in the back-end. The GBT module shown in blue rectangle in the figure 9 is for communication interface. It is based on the CERN GBT-FPGA project with some improvements, like separating GBT firmware from transceiver IP (Intellectual Property) block and using a fast clock for GBT encoding to reduce the link latency [19]. The GBT protocol has a line rate of 4.8 Gb/s with FEC encoding for radiation tolerance. Its data frame is 120 bits in 40 MHz clock domain. There are three GBT links between ZC706 boards and the FELIX. One GBT link is used to distribute clock and slow control commands from the FELIX. The other two links are used for FE-I4B commands and data communication, as well as sending back the monitoring data. In the FELIX, a PCIe interface module is implemented for communication between the FELIX hardware and the software in the host server. And some FE-I4B commands can also be generated inside FELIX firmware like trigger, calibration and etc.

The HitOr signals from the front and bottom IBL DC modules are used for trigger generation in the testbeam experiment [5]. The logic AND is implemented to suppress noise triggered events. In the FELIX, the FE-I4B commands come from either software tools or an inner command generator inside firmware. In the FE-I4B calibration tests, FELIX software tools are used to send FE-I4B commands. In the testbeam experiments, FELIX generates and distributes trigger commands after receiving HitOr signal from front-end electronics to readout beam data. The delay time between trigger commands generation and receiving HitOr signal is configurable which should match the



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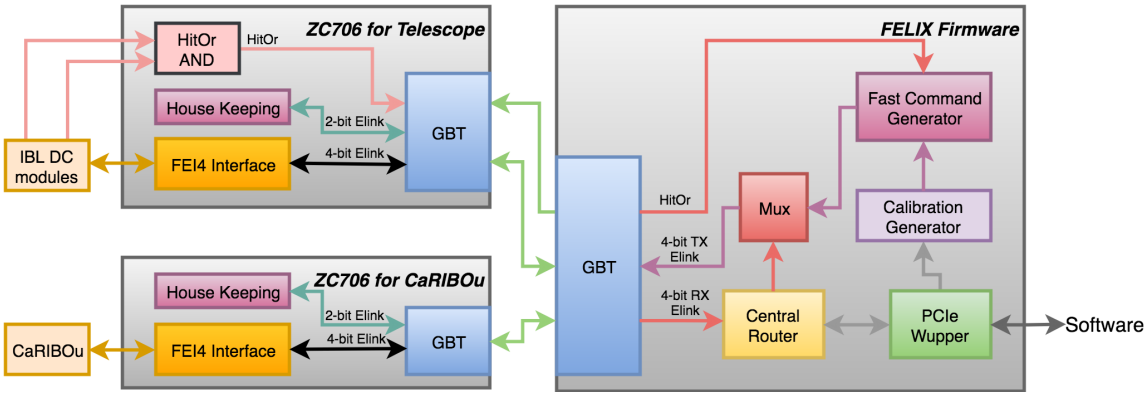


**Figure 9**. Functional block diagram of firmware.

trigger latency in the FE-I4B ASIC. The full trigger chain, including GBT link transmission, is latency fixed to get the appropriate timing information of the beam data.

The House Keeping module is for general slow control and monitoring of the whole readout system. The I2C bus in ZC706 boards is mapped to 2-bit data in the GBT 120-bit data frame. In this way, the front-end electronics can be configured through the FELIX, such as jitter cleaner Si5345 on Telescope FMC Card, power rails and bias voltages in the CaRIBOu system. The clock distribution scheme is shown in the figure 10. The recovered clock from the FELIX GBT link is used as the input for the Si5345 chip on the Telescope FMC Card. Its 240 MHz output channel is used as the reference clock for the data link in the ZC706-2. And 40 MHz output clocks are used as the system clock for two ZC706 boards respectively. The Si5324 on the ZC706-1 is used to generate reference clock of the data link on the ZC706-1.

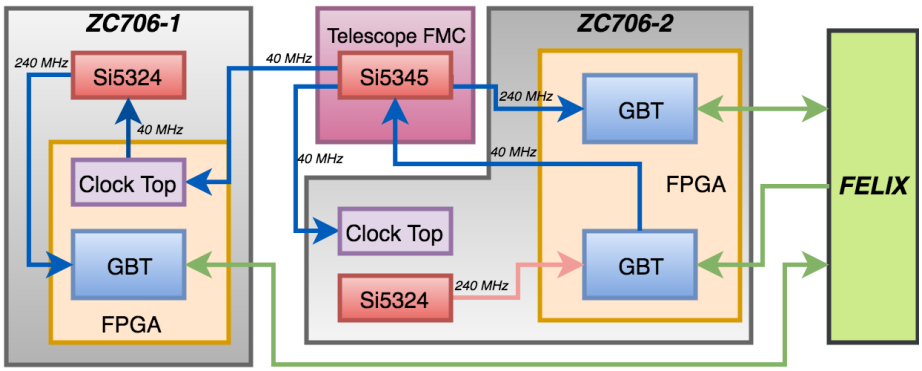


**Figure 10**. Clock distributation in the front-end electronics.

The FEI4 Interface module shown in the figure 9 communicates with FE-I4B chips on the IBL DC modules. Each FE-I4B chip uses one 4-bit Elink in the GBT frame for both to-host (from front-end to back-end) and from-host pathes. The phase relationship between the FE-I4B output data (160 Mb/s) and the system 160 MHz clock on the ZC706 board is uncertain, which also relies on the length of RJ45 cable used. The FEI4 Interface module includes a FSM (Finite State Machine) for FE-I4B output data synchronization. The phase of FE-I4B output data can be adjusted by using



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Idelay primitives in the ZC706 FPGA. Since FE-I4B chips send IDLE-P (10-bit) and IDLE-N (10-bit) commas repeatedly after initialization, a 20-bit parallel register is used to check the phase relationship, as shown in the figure 11. When the phase relationship between the system clock and the FE-I4B output data with FPGA Idelay is appropriate, the 20-bit check data is stable and constant. This calibration procedure can be executed automatically inside the ZC706 firmware.

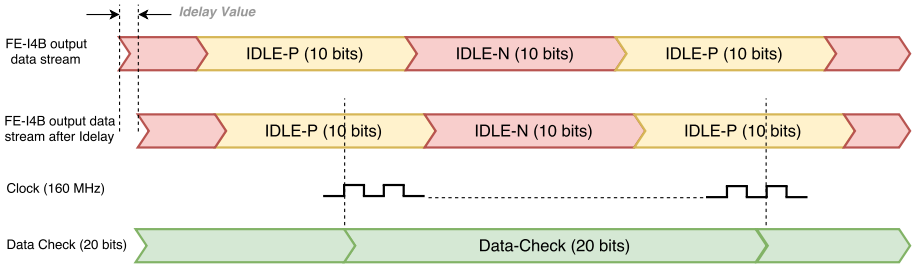


**Figure 11**. FE-I4B output data phase calibration.

## 6 Laboratory test results

The FE-I4B is fabricated in 130 *nm* CMOS process using thin gate oxide transistors for radiation hardness [11]. It hosts a pixel matrix of 336 rows by 80 columns. Each pixel size is 250 μm × 50 μm. Since each FE-I4B pixel has an independent, free running amplification stage with adjustable shaping, followed by a discriminator with adjustable threshold, the tuning test should be carried out to eliminate the threshold and feedback current variance between pixels. The tuning procedure includes global threshold scan, TDAC (Threshold DAC) scan, FDAC (Feedback current DAC) scan and TDAC rescan. The TDAC is an in-pixel 5-bit DAC for offset voltage that can be used to adjust pixel threshold. And the 4-bit FDAC is an in-pixel amplifer to adjust TOT (Time Over Threshold) information of input pulses. In all these scan tests, binary search is applied to reduce the time needed. The whole tuning test can be completed in less than 2 minutes. The tuning results of threshold distribution and TOT distribution are showed in figure 12 and figure 13 separately. The effective threshold deviation after tuning is around 77 electrons and TOT deviation is smaller than 1. These results are consistent to the specification of the FE-I4B chip [11]. This readout system can support readout of 12 FE-I4B chips in total. Since its data bandwidth is larger than FE-I4B output rate, it can support FE-I4B readout at its peak data rate, which is important to the testbeam experiment to have a high trigger rate.

The H35DEMO is an pixel demonstrator fabricated in the 350 *nm* HV-CMOS process [10]. It has four matrices: standalone matrix, analog matrix1, analog matrix2 and standalone cmos matrix. Each matrix has its own pads, bias block and configuration registers. And the H35DEMO pixels also include a small injection circuit for testing purpose. The injection test of two analog matrices has been carried out to verify the full readout chain of the H35DEMO together with the FE-I4B chip working properly. The test results are shown in the figure 14.



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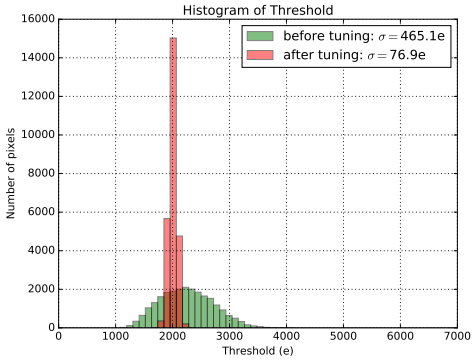


**Figure 12**. FE-I4B threshold distribution.

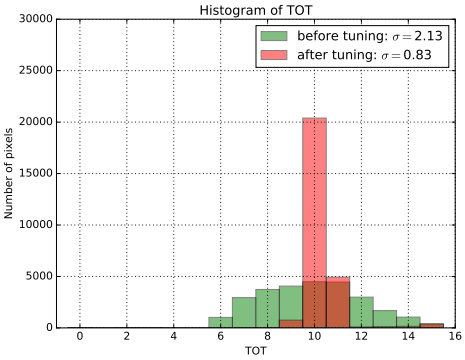


**Figure 13**. FE-I4B TOT distribution.

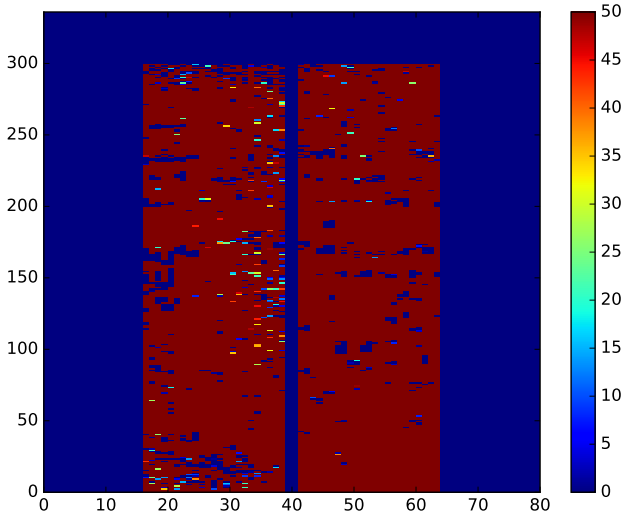

**Figure 14**. H35DEMO injection test.

## 7 Testbeam results

This FELIX based readout system has been deployed in the testbeam at the H8 beamline of the CERN Super Proton Synchrotron (SPS) in August 2017. It was used to control and readout all of the six IBL DC modules in the testbeam Telescope and the CaRIBOu system in the testbeam experiment. A photograph of the testbeam setup is shown in the figure 15. The CaRIBOu system with H35DEMO prototype was placed in a thermally insulated box equipped with cooling provided by a chiller and maintained at 25 °C or less during beam data taking. The FELIX was installed in a server PC in the control room. The trigger flow in testbeam is shown in the figure 16. A logic AND signal of the HitOr signals from the front and bottom IBL DC modules was generated in the ZC706, which was sent to the FELIX through GBT link for trigger commands generation. The FE-I4B HitOr signal is a hit bus output, which will be asserted when any of pixels is fired. After receiving



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this HitOr AND signal, the FELIX generates and distributes the trigger commands to both ZC706 boards in the front-end for testbeam data readout.

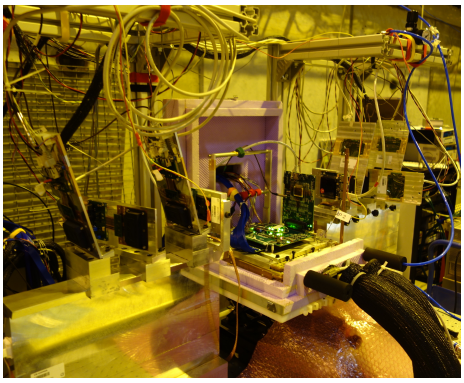

**Figure 15**. Testbeam setup at CERN.

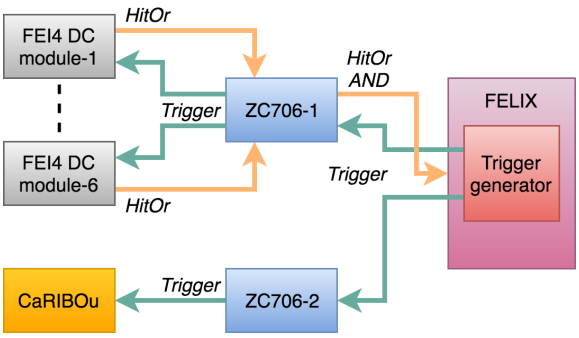


**Figure 16**. Trigger flow in testbeam.

In the testbeam experiment, beam particles passing the FE-I4B telescope planes create clusters in the sensors. The real-time heat map of one FE-I4B chip in the testbeam Telescope is shown in the figure 17. The spot area in the middle are regions for clusters. These generated clusters are spatially correlated between the individual planes. Correlations can be identified as straight lines in a histogram which is filled with all possible pairs of x and y direction in two neighbouring planes. The correlation plot of two FE-I4B planes is shown in the figure 19. It means this readout system can work properly and reliably without any event data lost. The testbeam data of H35DEMO in the CaRIBOu system is shown in the figure 18. Its two analog matrice beam data were readout via FE-I4B chips. As this readout system is able to readout all of the FE-I4B output data at full speed (160 Mb/s for each FE-I4B chip), it can support high trigger rate. In the testbeam experiment, the trigger rate was about 100 kHz. These test results demonstrate the FELIX is capable of FE-I4B testbeam Telescope and CaRIBOu system readout with high trigger rate in the testbeam experiment.

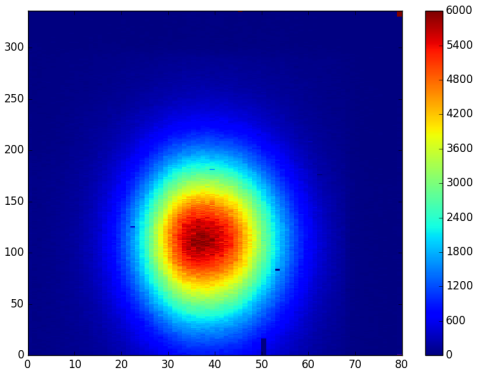


**Figure 17**. FE-I4B Telescope testbeam data.

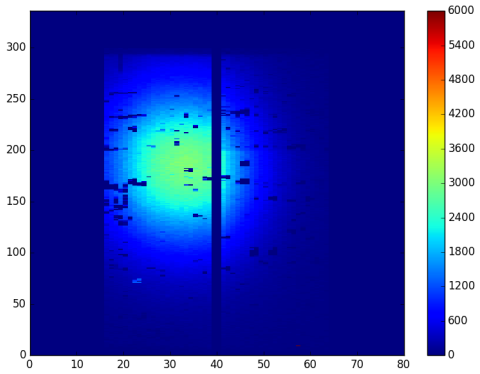


**Figure 18**. H35DEMO testbeam data.

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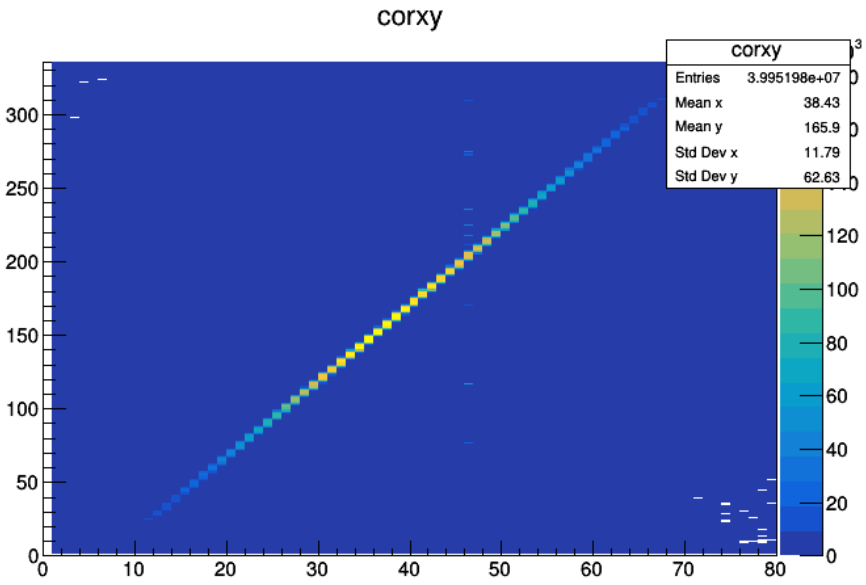


**Figure 19**. XY correlation of two FE-I4B telescope planes.

## 8 Conclusion

The FELIX based readout system has been developed for control and readout of the FE-I4B testbeam Telescope and CaRIBOu system in the testbeam experiment. An interface board of Telescope FMC Card has been designed for communication between the FE-I4B IBL DC modules in testbeam Telescope and the ZC706 board. The laboratory test results show that the FELIX based readout system can support FE-I4B tuning test and H35DEMO readout. This DAQ system was deployed successfully in the testbeam at the CERN SPS in August 2017. It has been proved to be effective to readout the testbeam data with high trigger rate.

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